TENTATIVE

Kaohsiung Opto-Electronics Inc.

FOR MESSRS :

DATE : Jul. 14th ,2010

TECHNICAL DATA

TX31D16VM2BAA

Contents

ACCEPTED BY:_____

PROPOSED BY:

2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 12.3" HSXGA of 8:3 format of amorphous silicon TFT. The pixel format is vertical stripe and sub pixels are arranged as R(red), G(green), B(blue) sequentially .This display is RoHS compliant , and COG (chip on glass) technology and CCFLbacklight are applied on this display.

Part Name	TX31D16VM2BAA
Module Dimensions	314.0(W) mm x 110.0(H) mm x 110 (D) mm
LCD Active Area	300.50(W) mm x 93.44(H) mm
Pixel Pitch	0.228(W) mm x 0.228(H) mm
Resolution	1024 x 3(RGB)(W) x 310(H) dots
Color Pixel Arrangement	R, G, B Vertical stripe
LCD Type	Transmissive Color TFT; Normally Black
Display Type	Active Matrix
Number of Colors	16.7M Colors (6-bit RGB)
Backlight	CCFL, 2pc Side-light type (U shape)
Weight	430 g
Interface	LVDS ; 20 pins
Power Supply Voltage	3.3V for LCD;
Viewing Direction	Super Wide Version (In Plane Switching)

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	4.0	V	-
Input Voltage of Logic	V_I	-0.3	V_{DD}+0.3	V	Note 1
Operating Temperature	T_{op}	-30	80	C	Note 2
Storage Temperature	T_{st}	-40	90	C	Note 2

Note 1: The rating is defined for the signal voltages of the interface such as CLK and pixel data pairs.

Note 2: The maximum rating is defined as above based on the chamber temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25 C .
- Operating under high temperature will shorten LED lifetime.

5. ELECTRICAL CHARACTERISTICS

5.1 LCD CHARACTERISTICS

T_a 25 C, Vss 0V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-	3.0	3.3	3.6	V	-
Differential Input Voltage for LVDS Receiver Threshold	V_I	"H" level	-	-	+100	mV	Note 1
		"L" level	-100	-	-		
Power Supply Current	I_{DD}	V_{DD}-V_{SS} =3.3V	-	520	620	mA	Note 2,3
Frame Frequency	f_{Frame}	-	55	60	65	Hz	-
CLK Frequency	f_{CLK}	-	39.6	43.2	46.8	MHz	

Note 1: VCM 1.2V is common mode voltage of LVDS transmitter and receiver. The input terminal of LVDS receiver is terminated with 100 .

IN+
100 LVDS
IN- Receiver

Note 2: An all white pattern is used when measuring I_{DD}. f_{Frame} is se t to 60Hz.

Note 3: 1.0 A fuse is applied in the module for I_{DD}. For display activation and protection purpose, power supply is recommended larger than 2.5A to start thedisplay and break fuse once any short circuit occurred.

5.2 BACKLIGHT CHARACTERISTICS

(2) BACK-LIGHT UNIT GND=0V

Item	Symbol	Min.	Max.	Unit	Note
Lamp Current	IL	-	7.0	mArms	1)
Lamp Voltage	VL	-	2000	Vrms	2)

Notes 1) To be measured at GND terminal side

2) The specification is applied at connector pins for back-light units .

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 30 minutes.
- The ambient temperature is 25 C .
- In the dark room less than 100 lx, the equipment has been set for the measurements as shown in Fig 6.1.

T_a 25 C, f_{Frame} 60 Hz, V_{DD} 3.3V

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White		-	0 , 0 , I_{LED}= 50mA/chain	400	500	-	cd/m^2	Note 1
Brightness Uniformity		-		70	-	-	%	Note 2
Contrast Ratio		CR		400	800	-	-	Note 3
Response Time (Rising + Falling)		Tr + Tf	0 , 0	-	25	-	ms	Note 4
NTSC Ratio		-	0 , 0	-	70	-	%	-
Viewing Angle		x	0 , CR 10	-	85	-	Degree	Note 5
		x	180 , CR 10	-	85	-		
		y	90 , CR 10	-	85	-		
		y	270 , CR 10	-	85	-		
Color Chromaticity	Red	X	0 , 0	0.57	0.62	0.67	-	Note 6
		Y		0.31	0.36	0.41		
	Green	X		0.25	0.30	0.35		
		Y		0.57	0.62	0.67		
	Blue	X		0.09	0.14	0.19		
		Y		0.02	0.07	0.12		
	White	X		0.25	0.30	0.35		
		Y		0.26	0.31	0.36		

Note 1: The brightness is measured from the panel center point, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \times 100\%$$

which is based on the brightness values of the 9 points in active area measured by BM-5 as shown in Fig. 6.2.

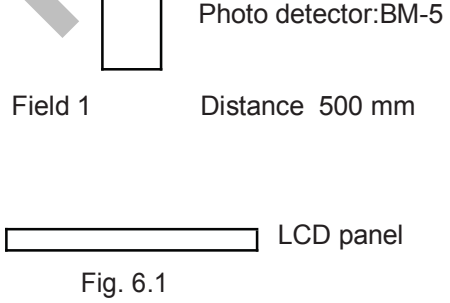


Fig. 6.1

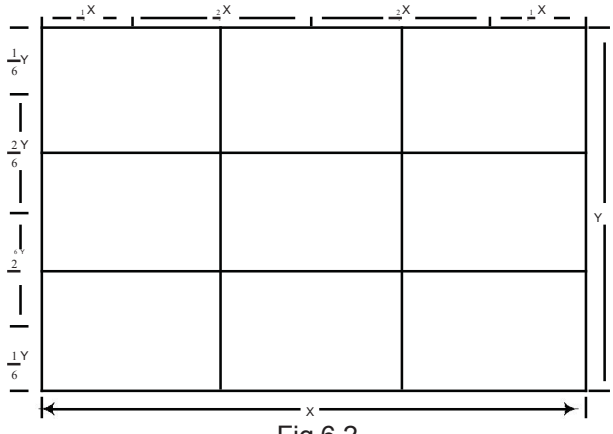
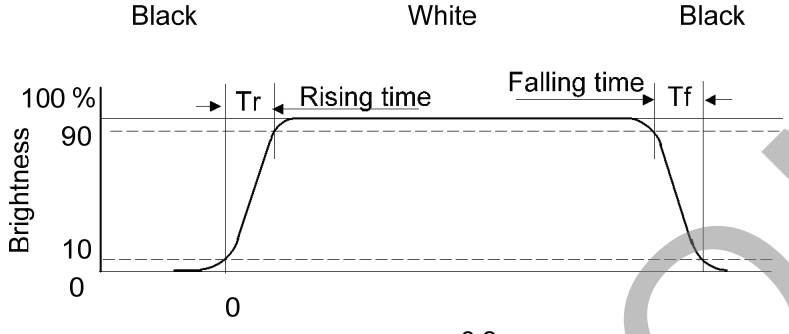


Fig 6.2

Note 3: The Contrast Ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 4: The definition of response time is shown in Fig. 6.3. The rising time is the period from 10% brightness to 90% brightness when the data is from black to white. Oppositely, Falling time is the period from 90% brightness rising to 10% brightness.



. 6.3

Note 5: The definition of viewing angle is shown in Fig. 6.4. Angle is used to represent viewing directions, for instance, 270 means 6 o'clock, and 0 means 3 o'clock. Moreover, angle is used to represent viewing angles from axis Z toward plane XY.

The display is super wide viewing angle version; 85° viewing angle can be obtained from each viewing direction.

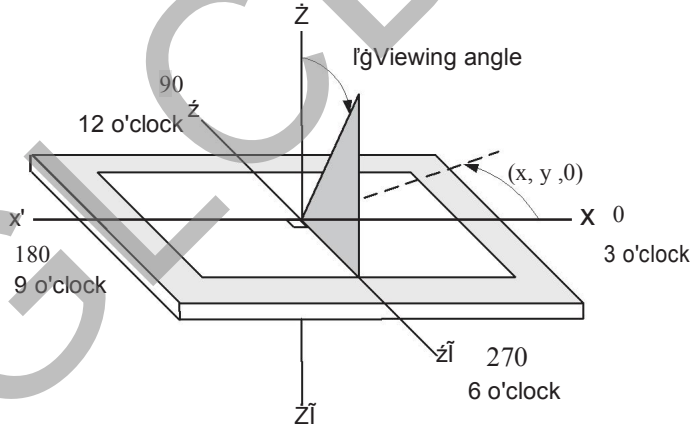
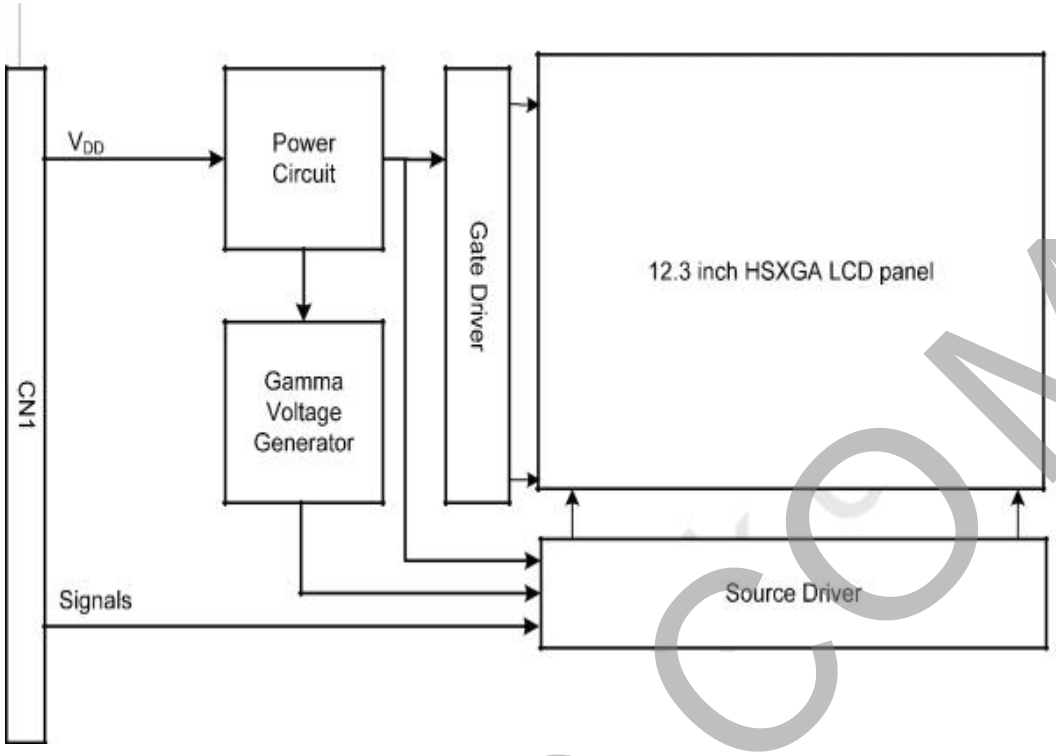


Fig 6.4

Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

7. BLOCK DIAGRAM



Color of wires f rom CCFL to CN2		
3	(GND)	: White
1	(VL)	: Pink

8. LCD INTERFACE

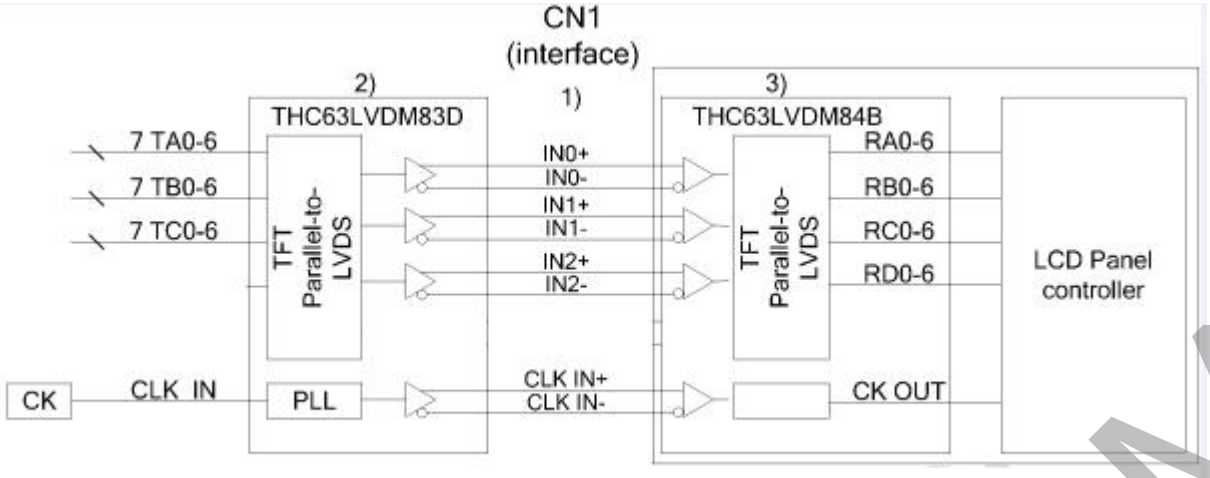
8.1 INTERFACE PIN CONNECTIONS

The display interface connector CN1 is FI-SEB20P-HF13E made by JAE and pin assignment is as below:

Pin No.	Signal	Signal	Pin No.	Signal	Signal
1	V_{DD}	Power Supply for Logic	11	IN2-	Pixel Data
2	V_{DD}		12	IN2+	
3	V_{SS}	GND	13	V_{SS}	GND
4	V_{SS}		14	CLK IN-	Pixel Clock
5	IN0-	Pixel Data	15	CLK IN+	
6	IN0+		16	GND	
7	V_{SS}	GND	17	NC	
8	IN1-	Pixel Data	18	NC	
9	IN1+		19	GND	
10	V_{SS}	GND	20	GND	

Note1: INn- and INn+ (n=0,1,2,3), CLK IN- and CLK IN+ should be wired by twist-pairs or side-by-side FPC patterns, respectively.

8.2 LVDS INTERFACE



Note 1: LVDS cable impedance should be 100 ohms per signal line when each 2-lines (+,-) is used in differential mode.

Note 2: The recommended transmitter, THC63LVDM83R, is made by Thine or equivalent, which is not contained in the module.

Note 3: The receiver built-in the module is THC63LVDM84B.

9.3 LVDS DATA FORMAT

8.4 TIMING CHART

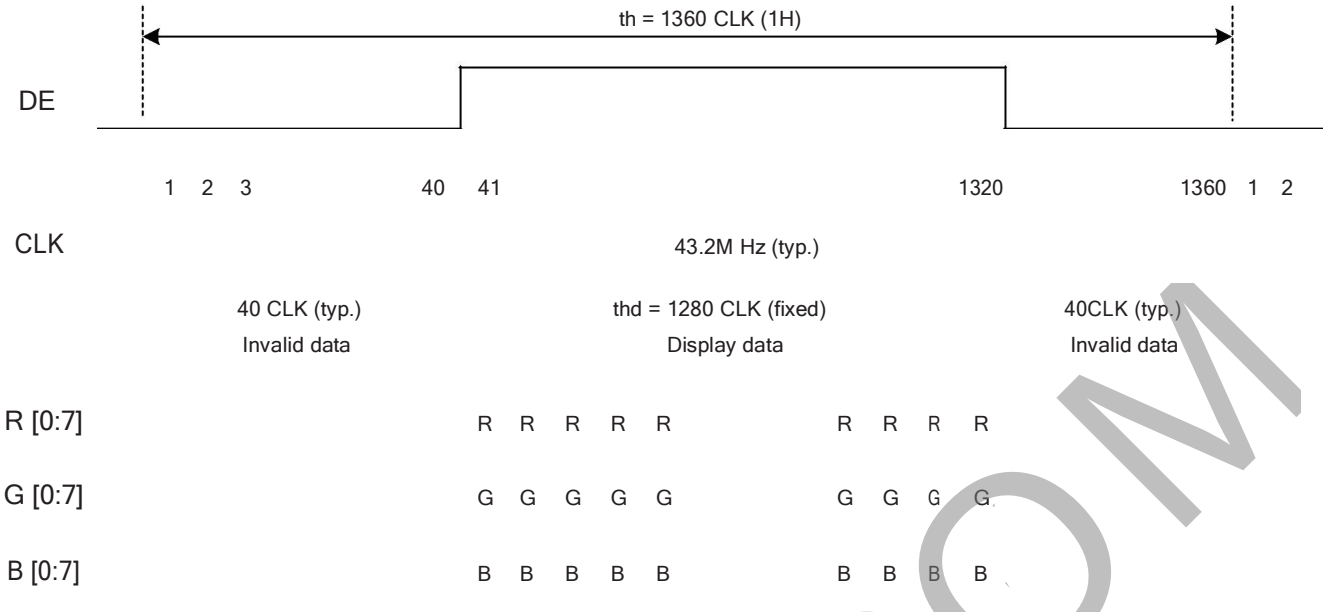


Fig. 8.1 Horizontal Timing

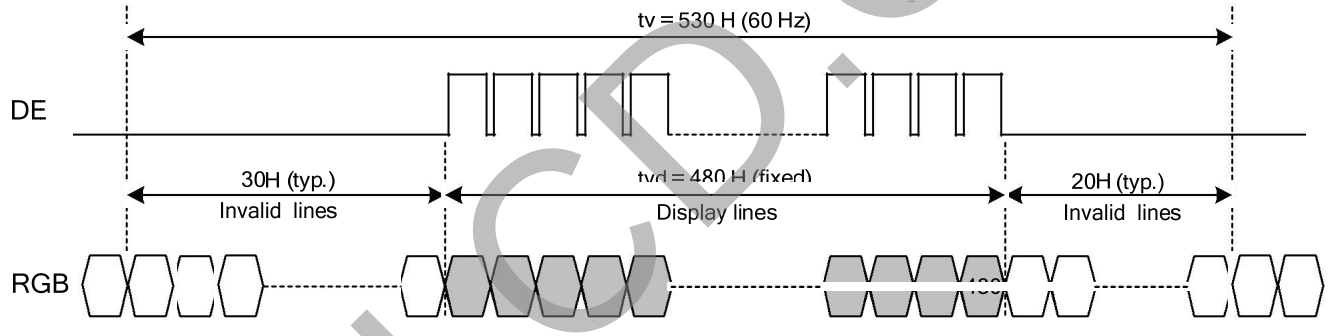


Fig. 8.2 Vertical Timing

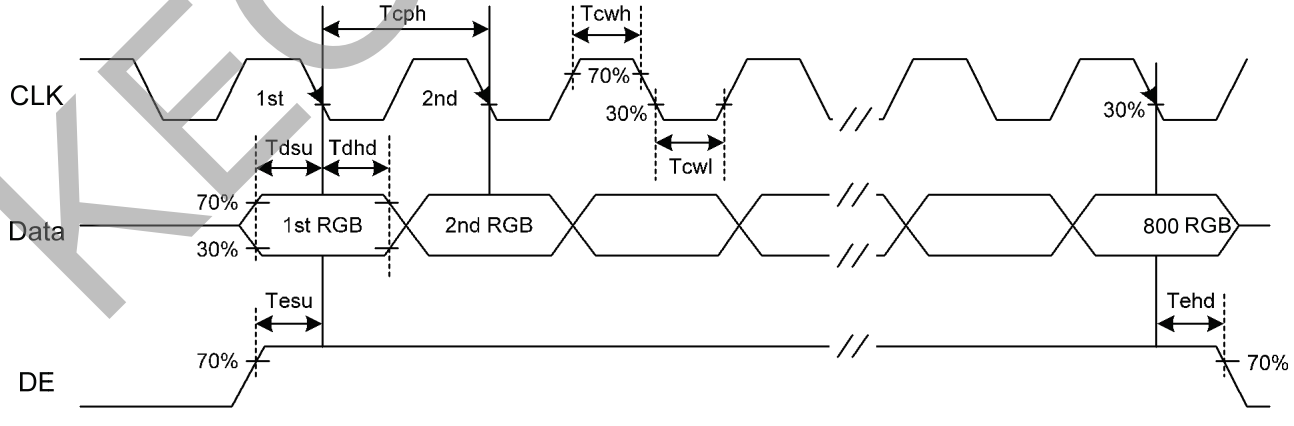


Fig. 8.3 Setup & Hold Time

8.5 TIME TABLE

The column of timing sets including minimum, typical, and maximum as below are based on the best optical performance, frame frequency (Vsync) = 60 Hz to define. If 60 Hz is not the aim to set, less than 66 Hz for Vsync is recommended to apply for better performance by other parameter combination as the definitions in section 5.1.

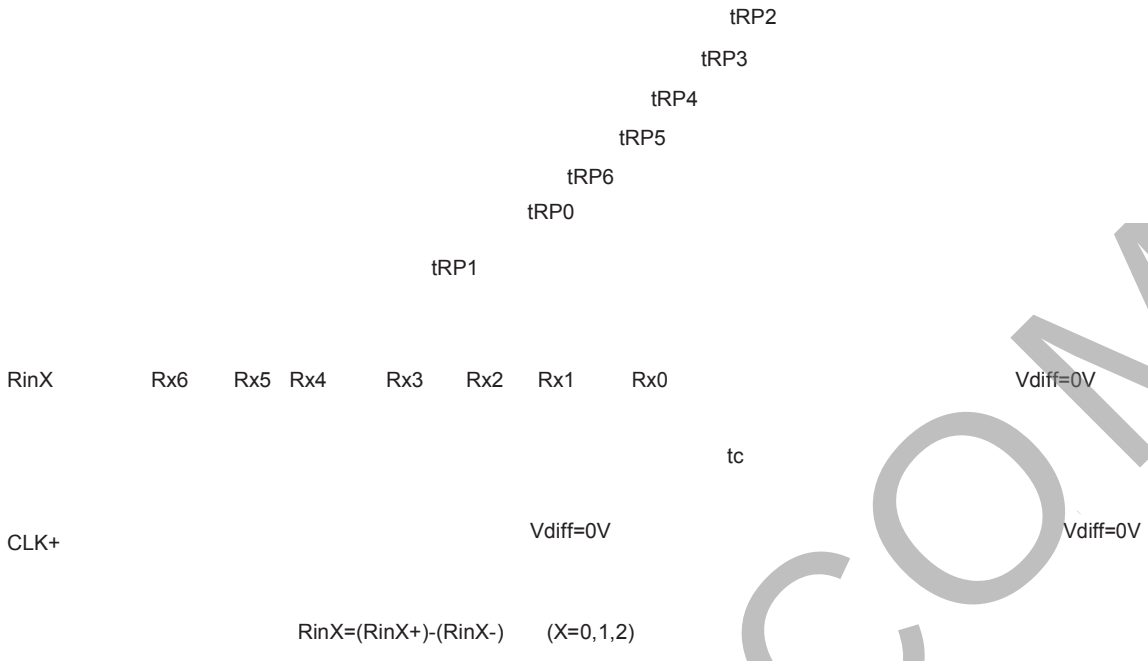
A. Horizontal and Vertical Timing

Item		Symbol	Min.	Typ.	Max.	Unit
Horizontal	CLK Frequency	fclk	39.6	43.2	48	M Hz
	Display Data	thd		1280		CLK
	Cycle Time	th	1320	1360	1400	
Vertical	Display Data	tvd		480		H
	Cycle Time	tv	500	530	555	

B. Setup and Hold Time

Item		Symbol	Min.	Typ.	Max.	Unit
CLK	Duty	Tcwh	40	50	60	%
	Cycle Time	Tcph	18.5	23	-	ns
Data	Setup Time	Tdsu	8	-	-	
	Hold Time	Tdhd	8	-	-	
DE	Setup Time	Tesu	8	-	-	
	Hold Time	Tehd	8	-	-	

8.6 LVDS RECEIVER TIMING

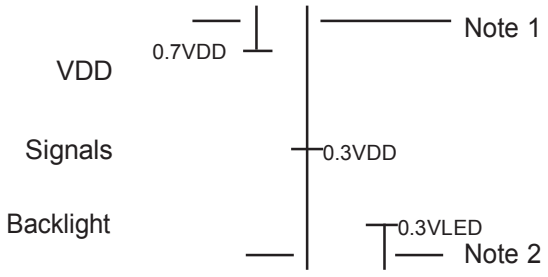


Item		Symbol	Min.	Typ.	Max.	Unit
CLK	Cycle frequency	1/t_{CLK}	39.6	43.2	48	MHz
RinX (X=0,1,2,3)	0 data position	tRP0	1/7* t_{CLK} -0.4	1/7* t_{CLK}	1/7* t_{CLK} +0.4	ns
	1st data position	tRP1	-0.4	0	+0.4	
	2nd data position	tRP2	6/7* t_{CLK} -0.4	6/7* t_{CLK}	6/7* t_{CLK} +0.4	
	3rd data position	tRP3	5/7* t_{CLK} -0.4	5/7* t_{CLK}	5/7* t_{CLK} +0.4	
	4th data position	tRP4	4/7* t_{CLK} -0.4	4/7* t_{CLK}	4/7* t_{CLK} +0.4	
	5th data position	tRP5	3/7* t_{CLK} -0.4	3/7* t_{CLK}	3/7* t_{CLK} +0.4	
	6th data position	tRP6	2/7* t_{CLK} -0.4	2/7* t_{CLK}	2/7* t_{CLK} +0.4	

9.7 DATA INPUT for DISPLAY COLOR

		Red Data								Green Data								Blue Data							
Input		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
color		MSB							LSB	MSB							LSB	MSB							LSB
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Basic	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Color	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Red	:	:	:	:	1	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Green	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

8.8 POWER SEQUENCE



Note 1: In order to avoid any damages, V_{DD} has to be applied before all other signals. The opposite is true for power off where V_{DD} has to be remained on until all other signals have been switch off. The recommended time period is 1 second. Hot plugging might cause display damage due to incorrect power sequence, please pay attention on interface connecting before power on.

Note 2: In order to avoid showing uncompleted patterns in transient state. It is recommended that switching the backlight on is delayed for 1 second after the signals have been applied. The opposite is true for power off where the backlight has to be switched off 1 second before the